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A Fuzzy Logic Controller for Enhancing the Transient Stability of 48-Pulse Inverter Based SSSC

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Abstract: The Static Synchronous Series Compensator (SSSC) is one of the recently developed Flexible AC Transmission System (FACTS) devices. In this paper, the SSSC is realized using a 48-pulse voltage source inverter. Fuzzy logic controllers are designed to operate the SSSC in the automatic power flow control mode. The parameters of the fuzzy controllers are varied widely by a suitable choice of membership functions and parameters in the rule base. The effectiveness of the fuzzy controllers is tested on a single machine infinite bus power system operating with a SSSC for a variety of transient disturbances and variation of operating point.

Keywords: Flexible AC transmission system, Fuzzy logic controller, Multi-pulse inverter, PI controller, Static synchronous series compensator.

1. INTRODUCTION

In recent years, it has become more difficult to construct new generation facilities and transmission lines due to energy and environmental problems. Hence it is advisable to enhance the power transfer capability of the existing transmission lines instead of constructing new one. Flexible AC transmission systems (FACTS) provide proven technical solutions to address these new operating challenges [1-3]. The static synchronous series compensator (SSSC) is one of the FACTS controllers connected in series with the transmission line is used to control the power flow in it without generating classical network resonance and oscillations [4].

High performance and cost effective high power voltage source inverters (VSI) are a prerequisite for the realization of SSSC. Since conventional two-pulse inverters are not available with higher ratings, multipulse inverters [5] with higher operating range are used to cater the need in SSSC. These multi-pulse inverters can be operated at lower switching frequencies, generating symmetrical output voltages having very low harmonic components.

The power converters which are the main elements in FACTS devices have complex models in which the Proportional-Integral-Derivate (PID) family of controllers failed to perform satisfactorily under parameter variations, non-linearity, load disturbances, etc [6, 7]. Moreover precise linear mathematical models are mandatory for Proportional-Integral (PI) controllers. Fuzzy logic controllers (FLC) does not need accurate mathematical model and are able to compensate the effects of uncertainties, disturbances and unmodelled system dynamics. Hence in this paper a closed loop control scheme using FLC has been developed for operating the SSSC in its most powerful control mode namely automatic power flow control mode. The performance of SSSC is verified on a single machine infinite bus power system subjected to wide range of operating conditions like faults and load variations.

2. STATIC SYNCHRONOUS SERIES COMPENSATOR

The SSSC is a power electronic-based synchronous voltage source that generates three phase ac voltages of controllable magnitude and phase angle. This voltage, which is injected in series with the transmission line, is almost in quadrature with the line current and hence emulates an equivalent inductive or capacitive reactance in series with the transmission line. When the series injected voltage leads the line current, it emulates an inductive reactance causing the power flow and the line current to decrease. When the line current leads the injected voltage it emulates a capacitive reactance thereby enhancing the power flow over the line. The basic schematic diagram of the static synchronous series compensator with its test system [8] is shown in Figure 1. The specifications of the test system are shown in Table 1.

The feeding network is represented by a Thevenin's equivalent circuit at bus B_1 where the voltage source is a 230×1.03 kV with a short circuit power level of 10,000 MVA and an X/R = 8. The SSSC is placed between two sections B_1 and B_2 of the transmission line as shown in Figure 1. The compensator is equipped with a source of energy, which helps in supplying or absorbing active power to or from the transmission line along with the control of reactive power flow.

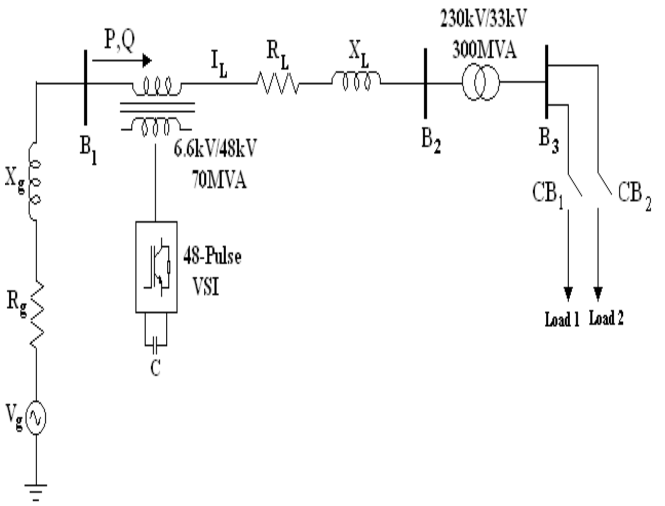


Figure 1. Schematic diagram of SSSC

Table 1. Specifications of the test system.

Parameters	Values
Rated Voltage	230 KV
MVA SC	10×10^3 MVA
Resistance	0.1 pu
Reactance	0.3 pu
Base Voltage	230 kV
Transmission line X_L	0.25 pu
Transmission line R_L	0.05 pu
DC Voltage	1 kV
Rated Power	70 MVAR
Capacitance	20 mF
Series Transformer-Rated Voltage	6.6 kV/48 kV
Series Transformer-Rated Power	70 MVA

3. 48-PULSE VOLTAGE SOURCE INVERTER

48-Pulse inverter can be used in high power FACTS controllers, without AC filters due to its high performance and low harmonic rate on the AC side. The schematic diagram of 48-pulse VSI is shown in Figure 2. 48-Pulse inverters are obtained by combining eight 6-Pulse VSIs with an adequate phase shifts between them. Each of the VSI needs a coupling transformer of which four of them require a Y-Y transformer with a turns ratio of 1:1 and the remaining four require a Δ-Y with a turns ratio of 1:√3. The output of the phase shifting transformers is connected in series to cancel out the lower order harmonics.

To create a 48-pulse waveform with a harmonic content in the order of m = 48r±1, (where r = 0, 1, 2...) the eight 6- pulse converter voltages need to be phase shifted. This is implemented by introducing appropriate phase shift in the phase shifting transformer and the gate pulse pattern of individual VSI. Table 2 shows the phase displacements applied to the gate pulse pattern of each VSI and the corresponding phase shifting transformer.

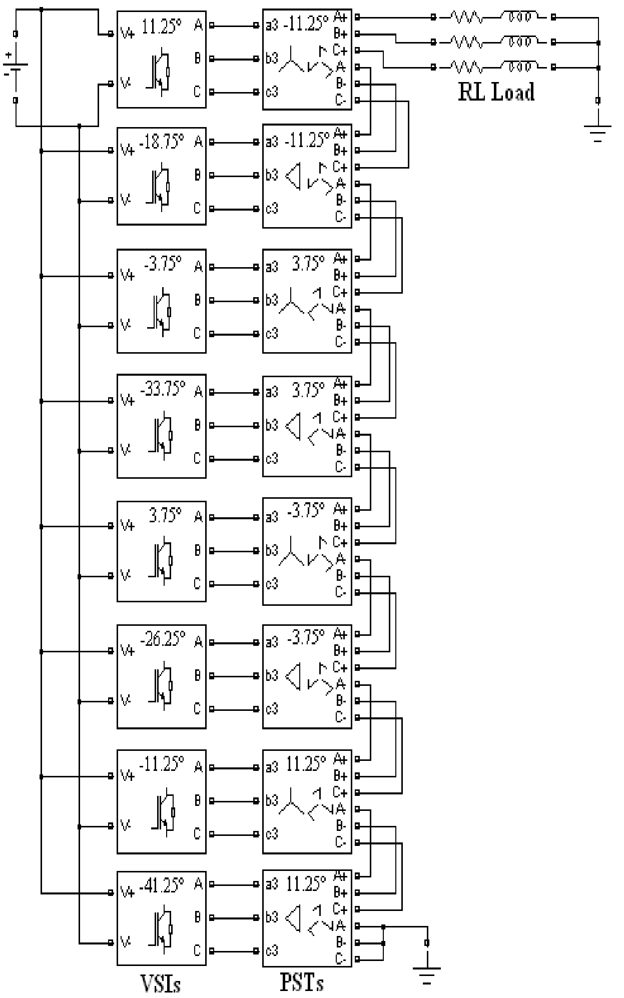


Figure 2. 48-pulse voltage source inverter

The instantaneous values of the phase-to-phase voltage $V_{ab}(t)$ and the phase-to-neutral voltage $V_{an}(t)$ of the 48-pulse inverter output voltage is expressed as

$$V_{ab_{48}}(t) = 8\sum_{m=1}^{\infty} V_{ab_m}\sin\left(m\omega t + 18.75^\circ m + 11.25^\circ i\right) \quad (1)$$

$$V_{an_{48}}(t) = \frac{8}{\sqrt{3}}\sum_{m=1}^{\infty} V_{an_m}\sin\left(m\omega t + 18.75^\circ m - 18.75^\circ i\right) \quad (2)$$

where

$$V_{ab_m} = \frac{4}{m\pi} V_{DC}\cos\frac{\pi}{6}m$$

$$V_{an_m} = \frac{4}{3\pi m} V_{DC}\left(1+\cos\frac{\pi}{3}m\right)$$

m = 48r ± 1, r = 0, 1, 2 …
i = 1, for positive sequence harmonics
i = -1, for negative sequence harmonics

The voltages v_{bc48} and v_{ca48} exhibit a similar pattern except phase shifted by 120° and 240° respectively. Similarly the phase voltages v_{bn48} and v_{cn48} are also phase shifted by 120° and 240° respectively.

Table 2. Phase displacement for a 48-pulse VSI

Coupling transformer	Gate pulse pattern	Phase shifting transformer
Y-Y	+11.25°	-11.25°
Δ-Y	-18.75°	-11.25°
Y-Y	-3.75 °	+3.75°
Δ-Y	-33.75°	+3.75°
Y-Y	+3.75°	-3.75°
Δ-Y	-26.25°	-3.75°
Y-Y	-11.25°	+11.25°
Δ-Y	-41.25°	+11.25°

4. CLOSED LOOP CONTROL SCHEME

The main function of the SSSC is to dynamically control the power flow over the transmission line. The control scheme proposed by Pradhan and Lehn [9] is based on the line impedance control mode in which the SSSC compensating voltage is derived by multiplying the current amplitude with the desired compensating reactance X_{qref}. Since it is difficult to predict X_{qref} under varying network contingencies, in the proposed scheme, this controller is modified as shown in Figure 3 to operate the static synchronous series compensator in the automatic power flow control mode [10]. In this mode the reference input to the controller are P_{ref} and Q_{ref}, which are to be maintained in the transmission line despite of system changes. The instantaneous power is obtained in terms of d-q quantities as:

$$P = \frac{3 v_d i_d}{2} \tag{3}$$

$$Q = \frac{3 v_d i_q}{2} \tag{4}$$

From equations (3) and (4) the required current references are calculated as follows:

$$I_{dref} = \frac{2P_{ref}}{3v_d} \tag{5}$$

$$I_{qref} = \frac{2Q_{ref}}{3V_d} \tag{6}$$

The line current I_{abc} and the line voltage V_{abc} are sensed at the point B_2 on the transmission line of Figure 1 and are converted into d-q components using Parks' transformation. The desired current references namely I_{dref} and I_{qref} are compared with actual current components I_d and I_q respectively and the error signals are processed in the FLC. This FLC is a nonlinear controller and not so sensitive to system topology, parameter and operating condition change as the conventional linear controller. These features make it attractive for power system applications [11,12]. The degree of membership function used for fuzzification and defuzzzification for both the fuzzy logic controllers are shown in Figure 4**.** The corresponding rules set for this process is shown in Table 3. Based on this rules set the required small displacement angle β to control the angle of the injected voltage with respect to the line current has been derived.

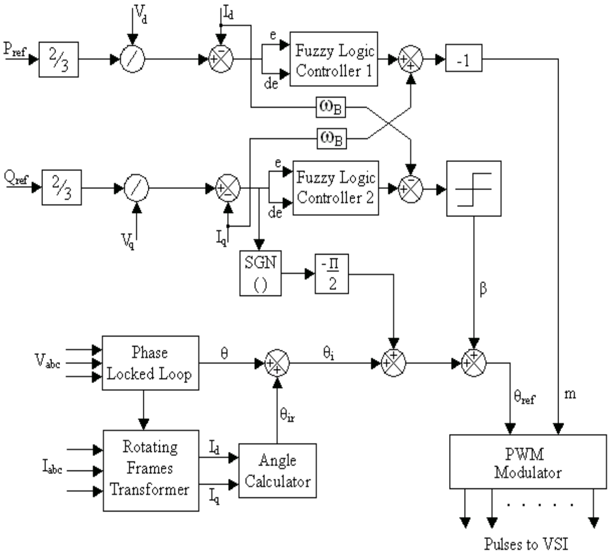


Figure 3. SSSC closed loop control scheme

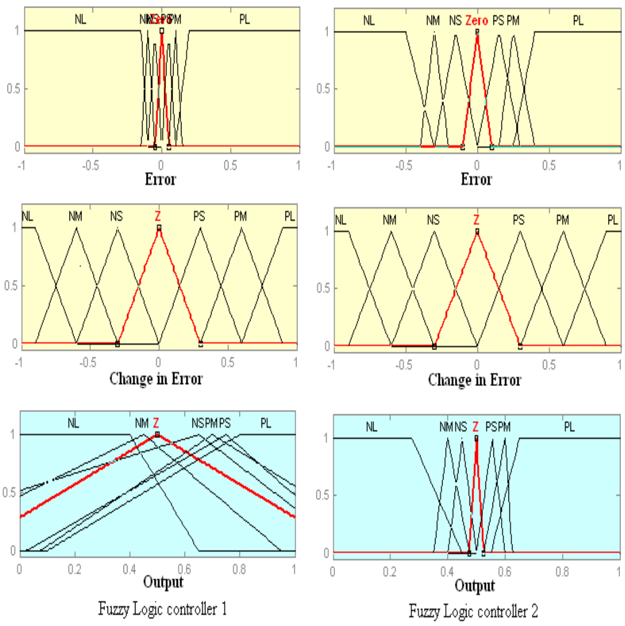


Figure 4. Membership function of error, change in error and output of FLCs

A phase locked loop (PLL) is used to determine the instantaneous angle θ of the three-phase line voltage V_{abc}. The current components I_d and I_q of the three phase line currents are used to determine the angle θ_{ir} relative to the voltage V_{abc}. Depending upon the instantaneous reactive power with respect to the desired value either π/2 is added (inductive) or subtracted (capacitive) with β. Thus the required phase angle is derived as $\theta_{ref} = \theta + \theta_{ir} + \beta \pm (\pi/2)$. The modulation index m derived from the active power control part of the circuit and the phase angle θ_{ref} are applied to the PWM modulator to generate the SSSC compensating voltage. Using θ_{ref} and m, the fundamental component of PWM inverter output voltage is obtained as follows:

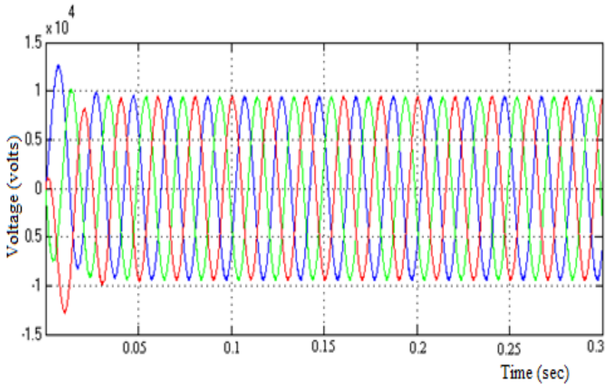
$$v_{sine} = m \sin\left(2\pi f t - \theta_{ref}\right) \tag{7}$$

Table 3. Rule Table of the Fuzzy logic controller

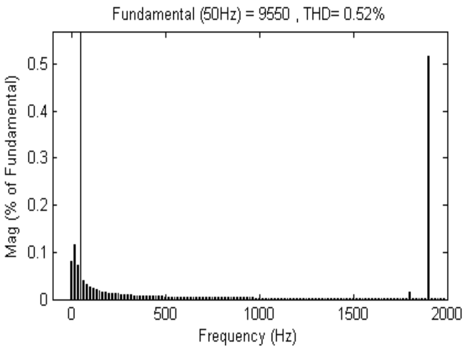
		Error						
		PL	**PM**	**PS**	**Z**	**NS**	**NM**	**NL**
Change in Error	**NL**	PL	PL	PL	PM	PM	PS	Z
	NM	PL	PL	PM	PM	PS	Z	NS
	NS	PL	PM	PS	PS	Z	NS	NM
	Z	PL	PM	PS	Z	NS	NM	NL
	PS	PM	PS	Z	NS	NM	NL	NL
	PM	PS	Z	NS	NM	NM	NL	NL
	PL	Z	NS	NM	NM	NL	NL	NL

5. SIMULATION RESULTS AND DISCUSSION

The 48-pulse inverter based SSSC is simulated using MATLAB/Simulink to analyse its operation. The various transient disturbances due to faults and load variations are created to study the performance of the fuzzy logic controller for SSSC. The VSI output voltage and the corresponding THD are shown in the Figures 5a and 5b.



(a). Output voltage



(b). THD

Figure 5. 48-Pulse VSI output voltage and its THD

After optimal tuning of the FLC load variation is applied to the test system. The initial load in the system is Load 1 with the ratings of 300 MW, 150 Mvar and is disconnected at time t= 0.2 s and Load 2 with ratings of 400 MW, 180 Mvar is connected to the system. The transmission line current is lagging the transmission line voltage as shown in Figure 6 whose power factor angle (ϕ) is clearly depicted in the Figure 7. Based on this angle and the amount of desired real and reactive power flow over the transmission line, the closed loop controller generates a modulating reference waveform to the PWM modulator with a modulation index (m) and the reference angle (θ_{ref}) as shown in Figures 8a and 8b respectively. This enables the VSI to generate a voltage of desired magnitude and phase angle, which is to be injected in series with the transmission line as shown in Figure 9. This series injected voltage lags the line current by an angle (δ) less than 90° as described in Figure 10 and thereby provides capacitive compensation.

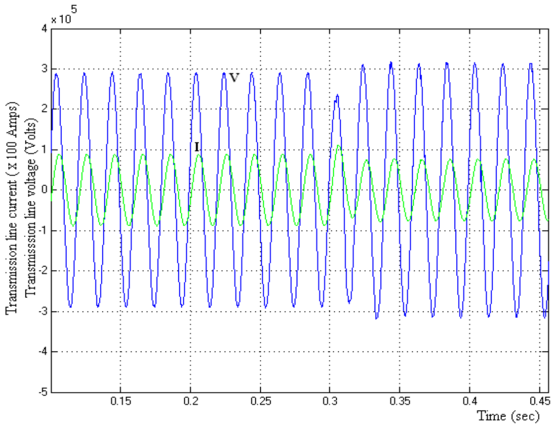


Figure 6. Transmission line voltage and current

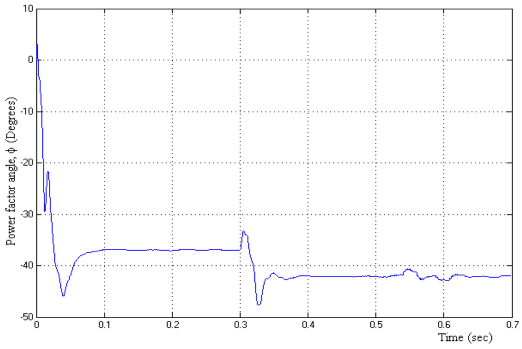
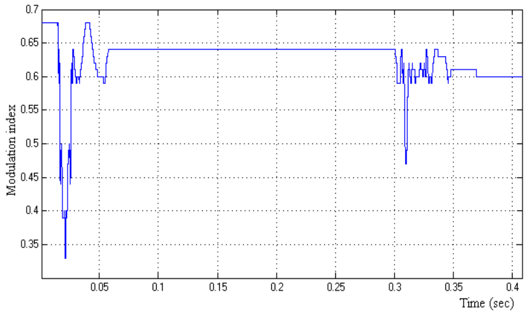
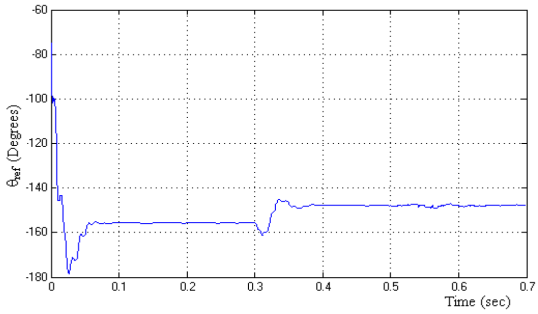


Figure 7. Variation of power factor angle



(a) Modulation index



(b) Reference angle to the PWM modulator

Figure 8. Inputs to the PWM modulator

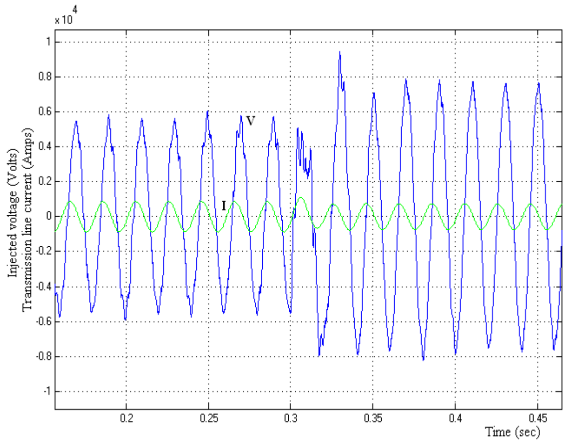


Figure 9. SSSC injected voltage and transmission line current

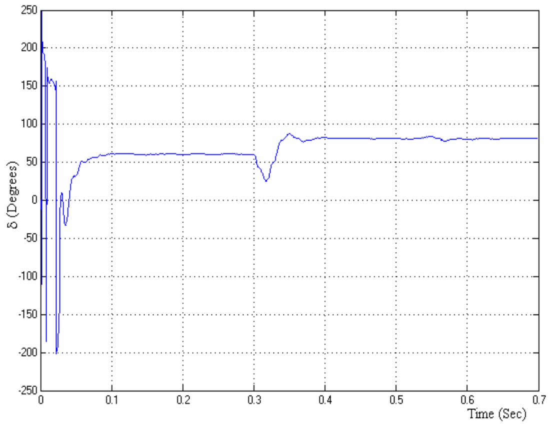


Figure 10. Angle of the transmission line current with respect to injected voltage

The magnitude and angle of this series injected voltage enables the active and reactive power of the transmission line to track the set reference values namely P_{ref} = 0.6 p.u and Q_{ref} = 0.25 p.u irrespective of load variations as depicted in Figure 11. However for the load variation given at t= 0.2 s the real and reactive power in the load side settles to a new reference value in the case of PI controller as shown in the Figure 12. This shows that the transient stability of the FLC controller is better than PI controller [7-9].

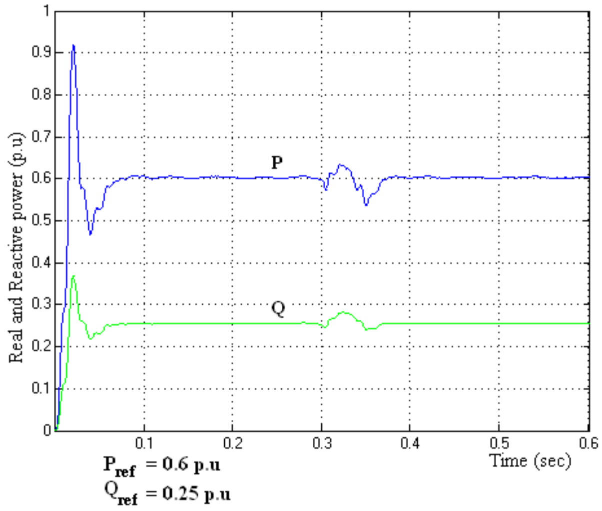


Figure 11. Real and Reactive power flow over the transmission line with FLC

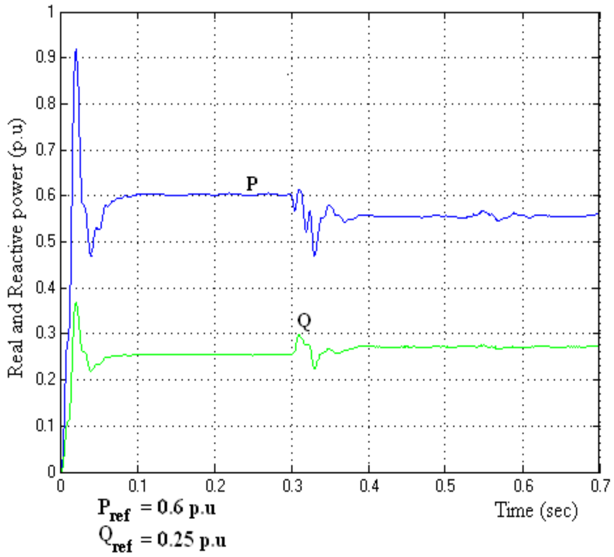


Figure 12. Reactive power flow over the transmission line with PI controller

The system performance is also verified when a three phase fault is applied at t = 0.3 s and cleared at t = 0.35 s as described in Figure 13. P and Q of the transmission line settle to the reference values within a small interval of time after the fault is cleared and this proves the transient stability of the proposed FLC for SSSC.

6. CONCLUSION

The dynamic performance of the proposed system is analysed with MATLAB/Simulink assuming that the SSSC is connected with the 230 kV transmission line of single machine infinite bus power system. The 48-pulse inverter generates symmetrical output voltages of desired magnitude and phase angle with very low harmonic components. A fuzzy logic based controller for SSSC has been developed to improve transient stability performance of the power system. To emphasize the merits of FLC, some comparisons have been made with the proportional-integral controller under certain load disturbances. It is inferred from the results that the FLC is a viable controller for the SSSC in order to maintain the real and reactive power flow over the transmission line to follow the set reference values under a variety of transient disturbances including high and low load conditions.

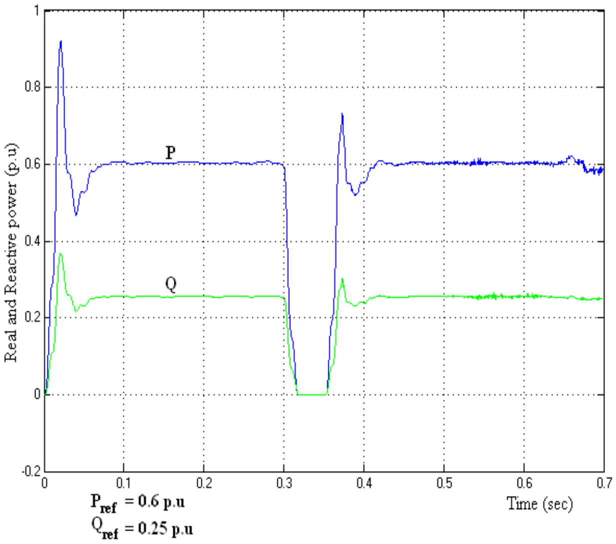


Figure 13. Real and reactive power flow over the transmission line for a three phase fault

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